

Fig. 1A

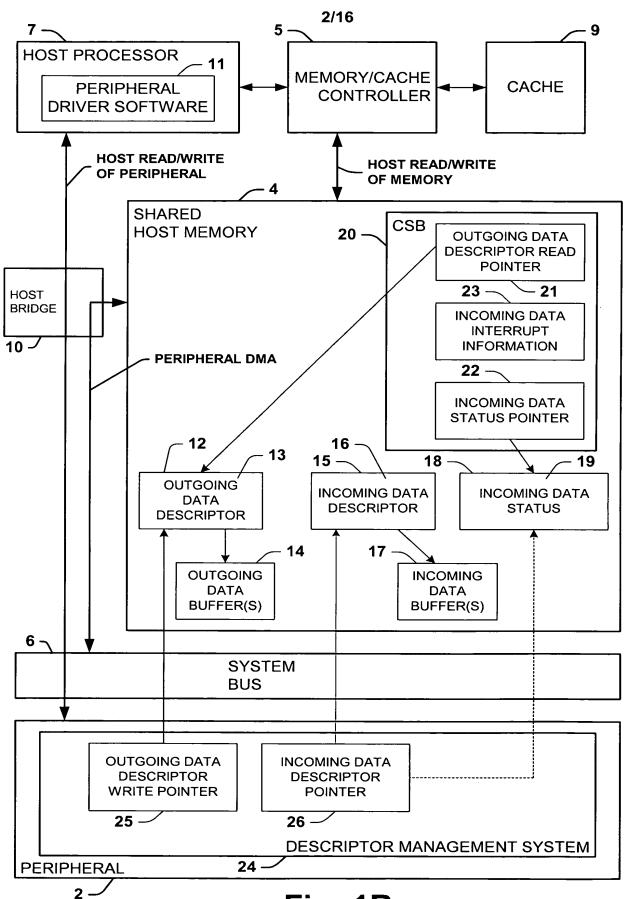


Fig. 1B

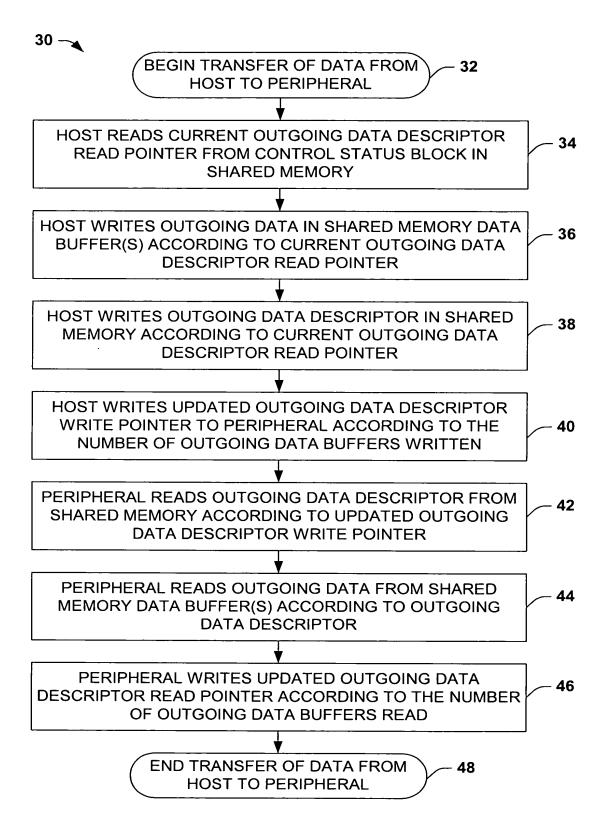


Fig. 1C

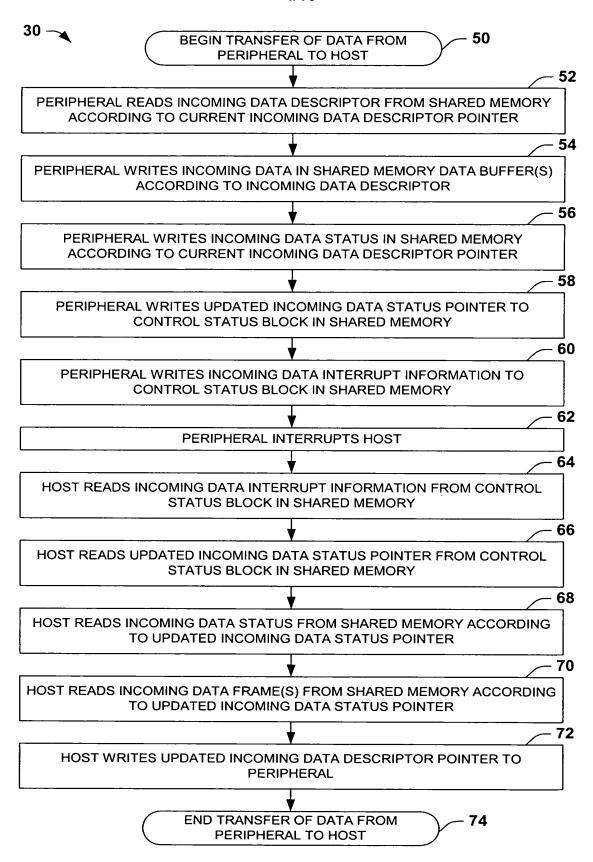
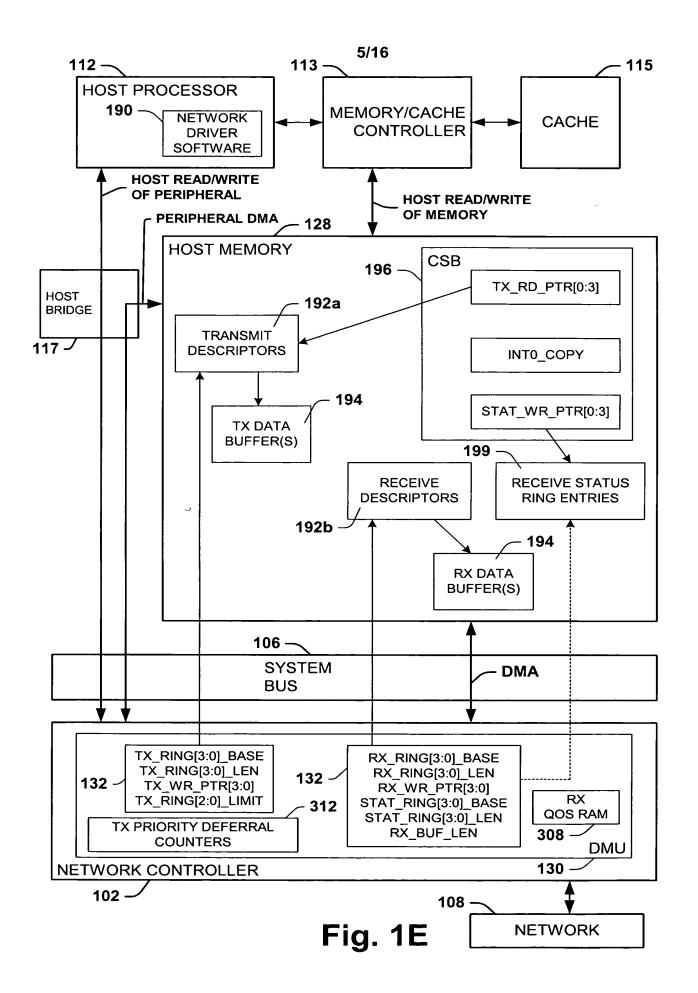


Fig. 1D



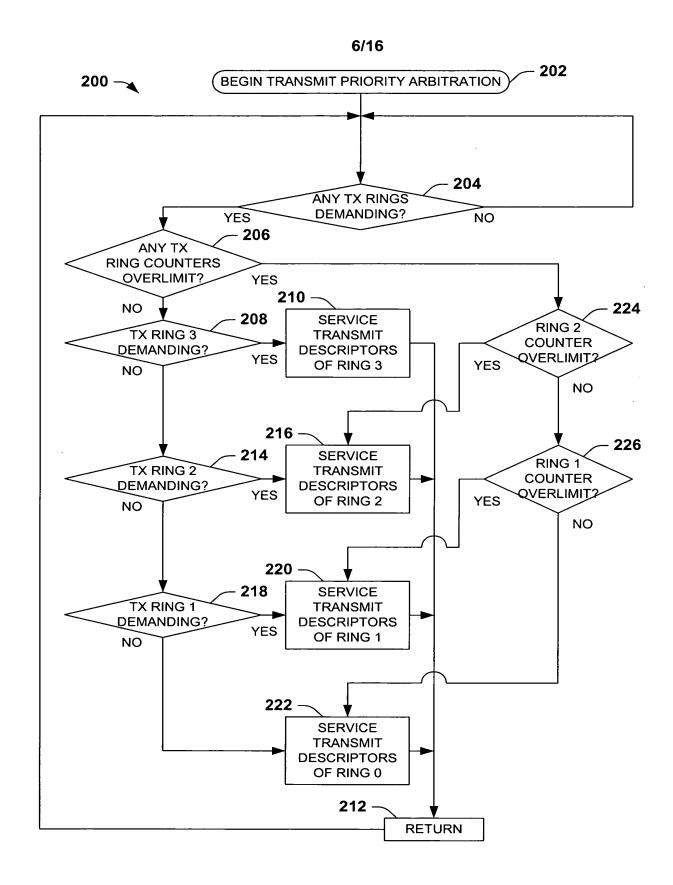


Fig. 1F

Fig. 1G

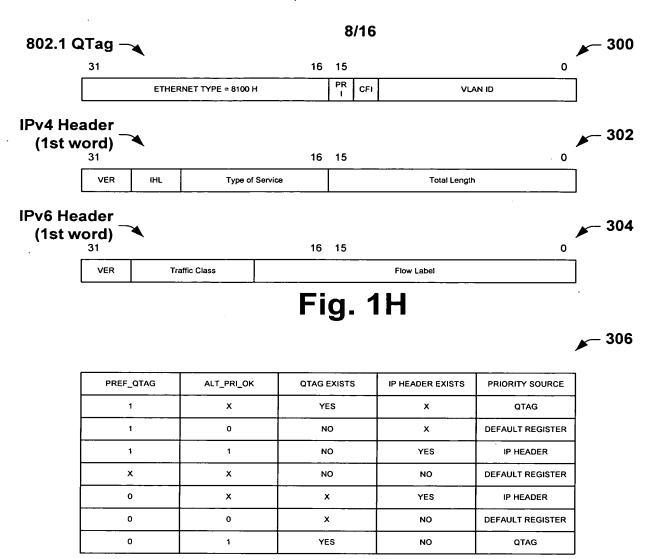


Fig. 11

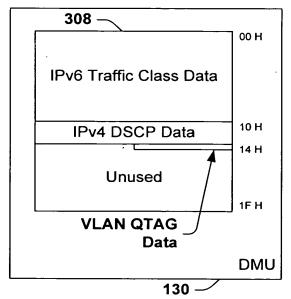
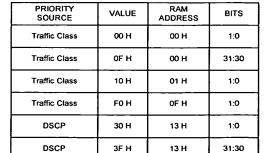


Fig. 1J



**▶** 310

14 H

14 H

1:0

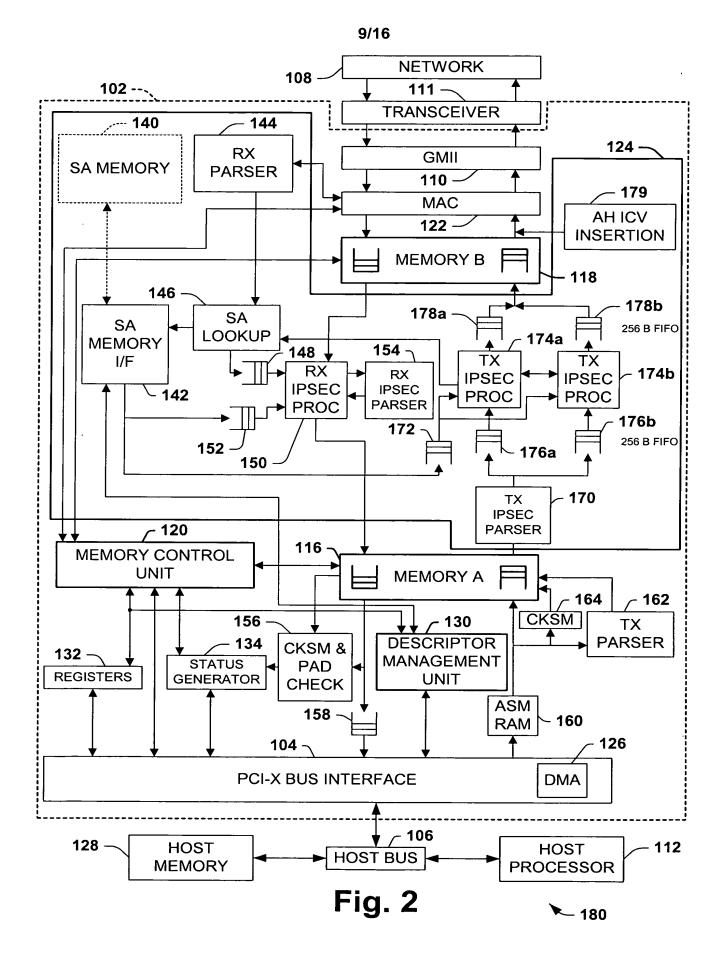
15:14

Fig. 1K

0

QTAG PRIORITY

QTAG PRIORITY



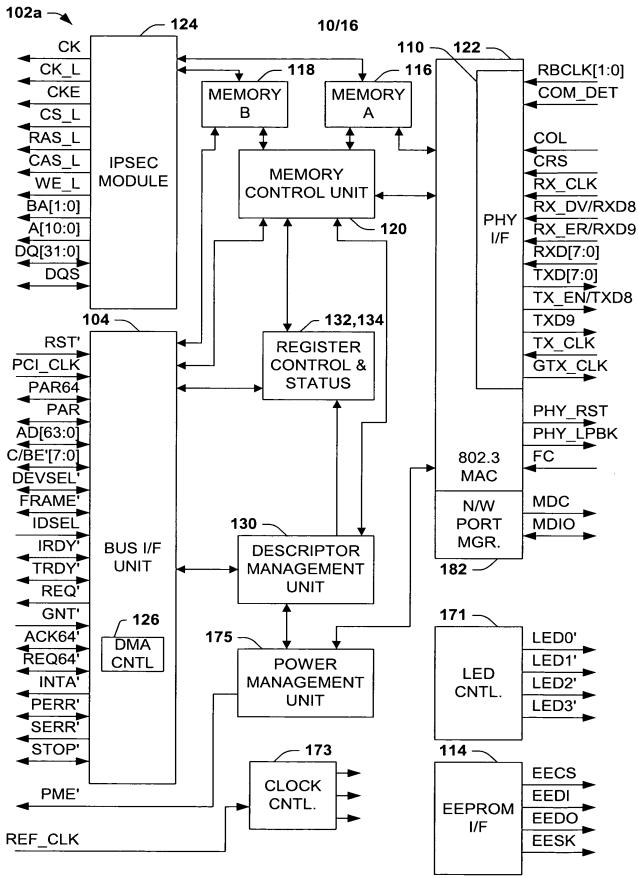


Fig. 3

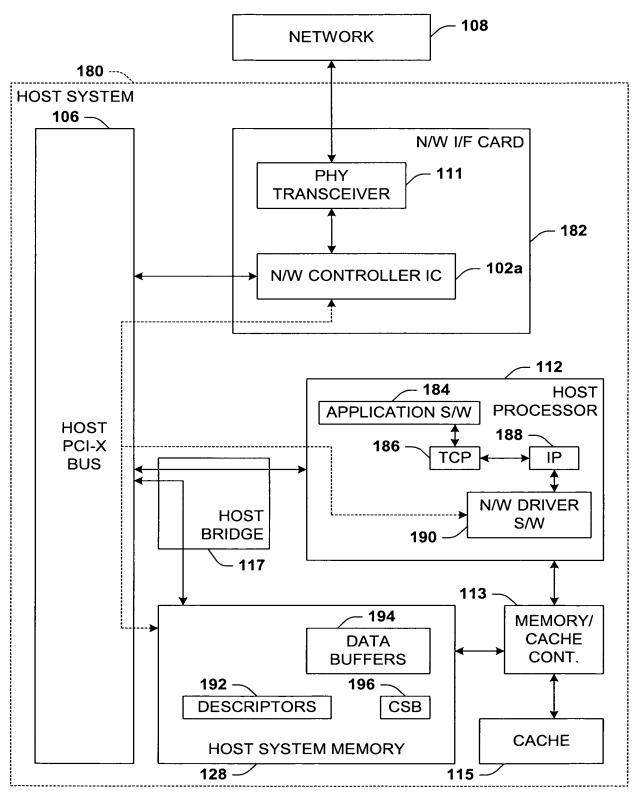


Fig. 4

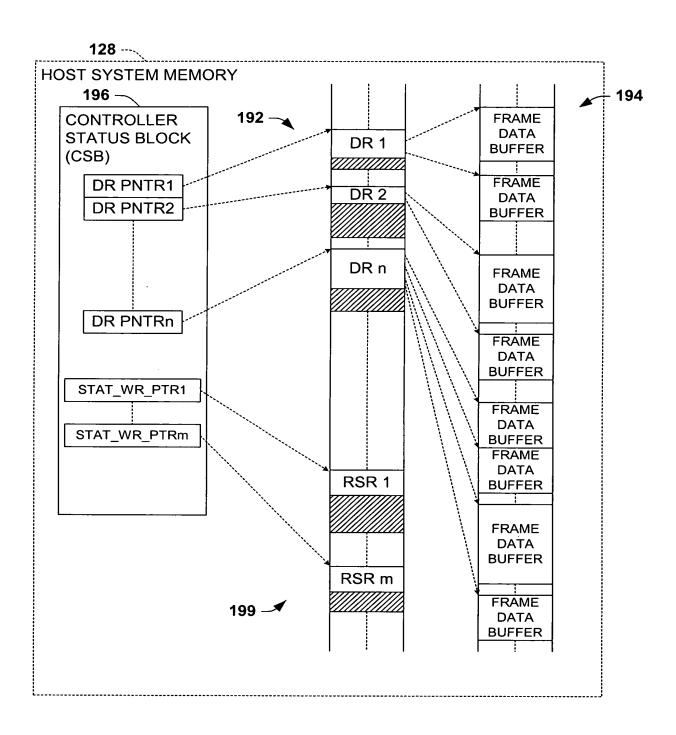


Fig. 5A

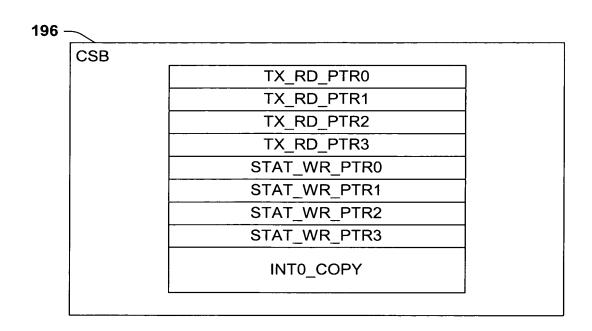


Fig. 5B

REGISTERS		
	RX_RING[3:0]_BASE	
	TX_RING[3:0]_BASE	1
	RX_RING[3:0]_LEN	1
	TX_RING[3:0]_LEN	7
	TX_WR_PTR[3:0]	7
	RX_WR_PTR[3:0]	7
	STAT_RING[3:0]_BASE	1
	STAT_RING[3:0]_LEN	1
	RX_BUF_LEN	1
	CSB_ADDR	7

Fig. 5C

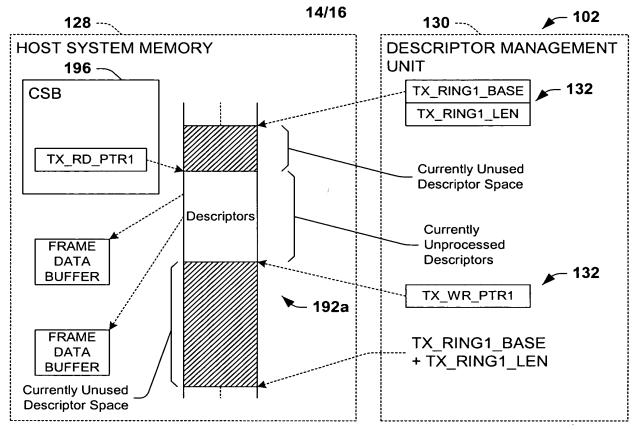
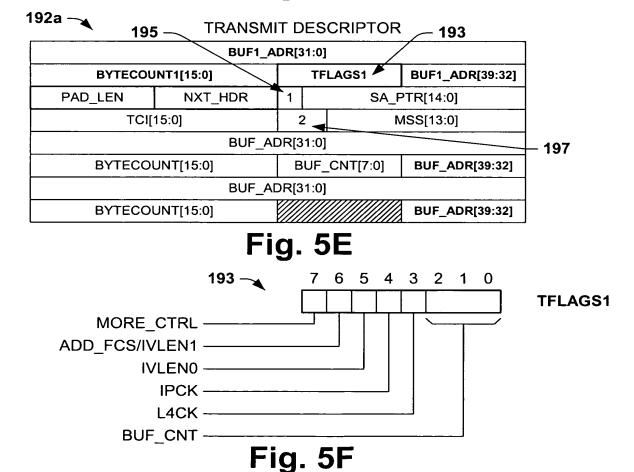


Fig. 5D



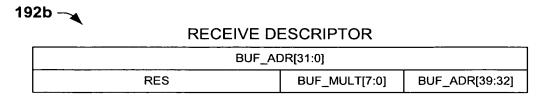


Fig. 5G

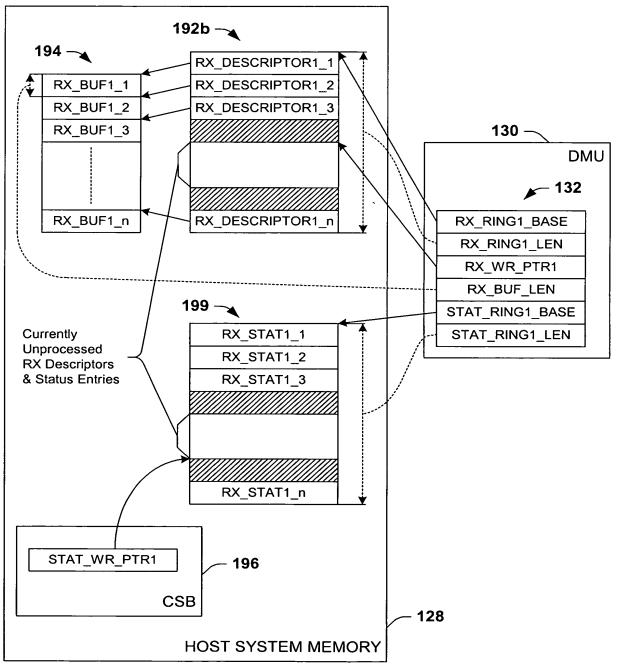
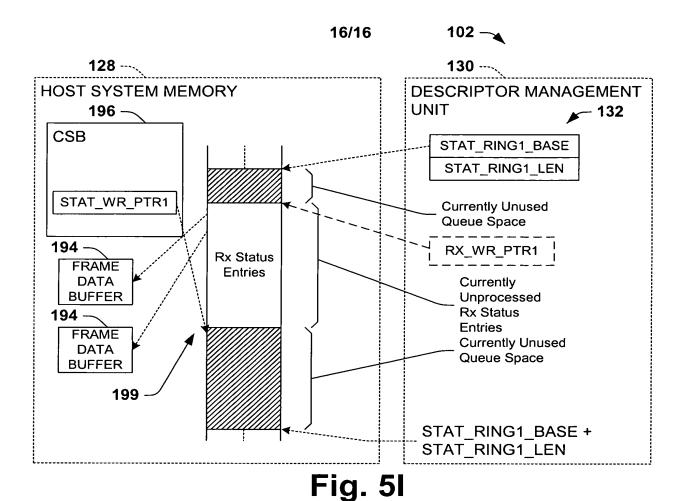


Fig. 5H



TCI[15:0] MCNT[15:0] **RECEIVE STATUS RING ENTRY** 199 -- RX\_ALIGN\_LEN[5:0] L4\_HEADER L4\_CK\_ERR - IP\_HEADER IP CK ERR RX MATCH[2:0] TT[1:0] - TRUNC - CRC - LEN ERR - PAD\_ERR ESPAH\_ERR - AH\_ERR **TUNNEL FOUND** - IPSEC\_STAT1[2:0] Fig. 5J